

**SPECIFICATION AMENDMENTS:**

Please replace paragraph [0069] with the following amended paragraph:

**[0001]** The lower breakdown voltage transistors 51 formed in the first region 50 are respectively disposed in device formation regions 53 isolated by a shallow trench isolation (STI) portion 52 formed in a surface of the silicon substrate 40. The STI portion 52 is formed by filling silicon oxide 55 in a shallow trench 54 (e.g., e.g., having a depth of about 4000Å) formed in the surface of the semiconductor substrate 40.

Please replace paragraph [0110] with the following amended paragraph:

**[0002]** As can be understood from Fig. 6, a hump phenomenon occurs in which a plurality of thresholds appear. This phenomenon becomes more remarkable as the back gate voltage BGV is increased. While Fig. 6 illustrates an exemplary characteristics of an N-channel high breakdown voltage transistor, a similar phenomenon is observed for a P-channel high breakdown voltage transistor. The hump phenomenon is caused by partial electrical conduction which occurs in the thinner film portion of the gate oxide film attributable to the recess 93. Where the thickness of the gate oxide film 80 is made uniform by eliminating the recess 93, the partial electrical conduction can be suppressed,

thereby suppressing the hump phenomenon. Thus, excellent static characteristics can be realized even if the back gate voltage is increased.